Control unit is combinational circuit.

Only input of control unit is opcode.

RTL: R-Type Instructions

Graphical user interface, application

Description automatically generated

Instruction Fetch Unit at the Beginning of Add

Diagram

Description automatically generated

The Single Cycle Datapath During Add

Diagram, schematic

Description automatically generated

Firstly, we will design ALU control which is responsible to send the right select signal to ALU.

Instruction Fetch Unit at the End of Add

Diagram

Description automatically generated

The Single Cycle Datapath During Load

Diagram, schematic

Description automatically generated

The Single Cycle Datapath During Store

Diagram, schematic

Description automatically generated

The Single Cycle Datapath During Branch

Diagram, schematic

Description automatically generated

Instruction Fetch Unit at the End of Branch

Diagram

Description automatically generated

**STEP 4: GIVEN DATAPATH RTL 🡪 CONTROL**

ALUop (which comes from control unit) is 10 so that ALU control will understand that the instruction is an R-type instruction so ALU control must check the function field which comes as an input.

Table

Description automatically generated

RegWr is 0 so MemtoReg is not important (X).

Truth Table for ALUControl

Table

Description automatically generated

8 bit input for ALU Control, we cant design output bits by Karnaugh Map.

Inputlara göre bakıyoruz. Örneğin C0 sadece en alt 2 satırda 1. En alt 2 satırı diğerlerinden ayıran özelliklere bakıyoruz.

c1’ = p1f2 ----> c1 = p1’ + f2’

Table, calendar

Description automatically generated

The ALU Control Block

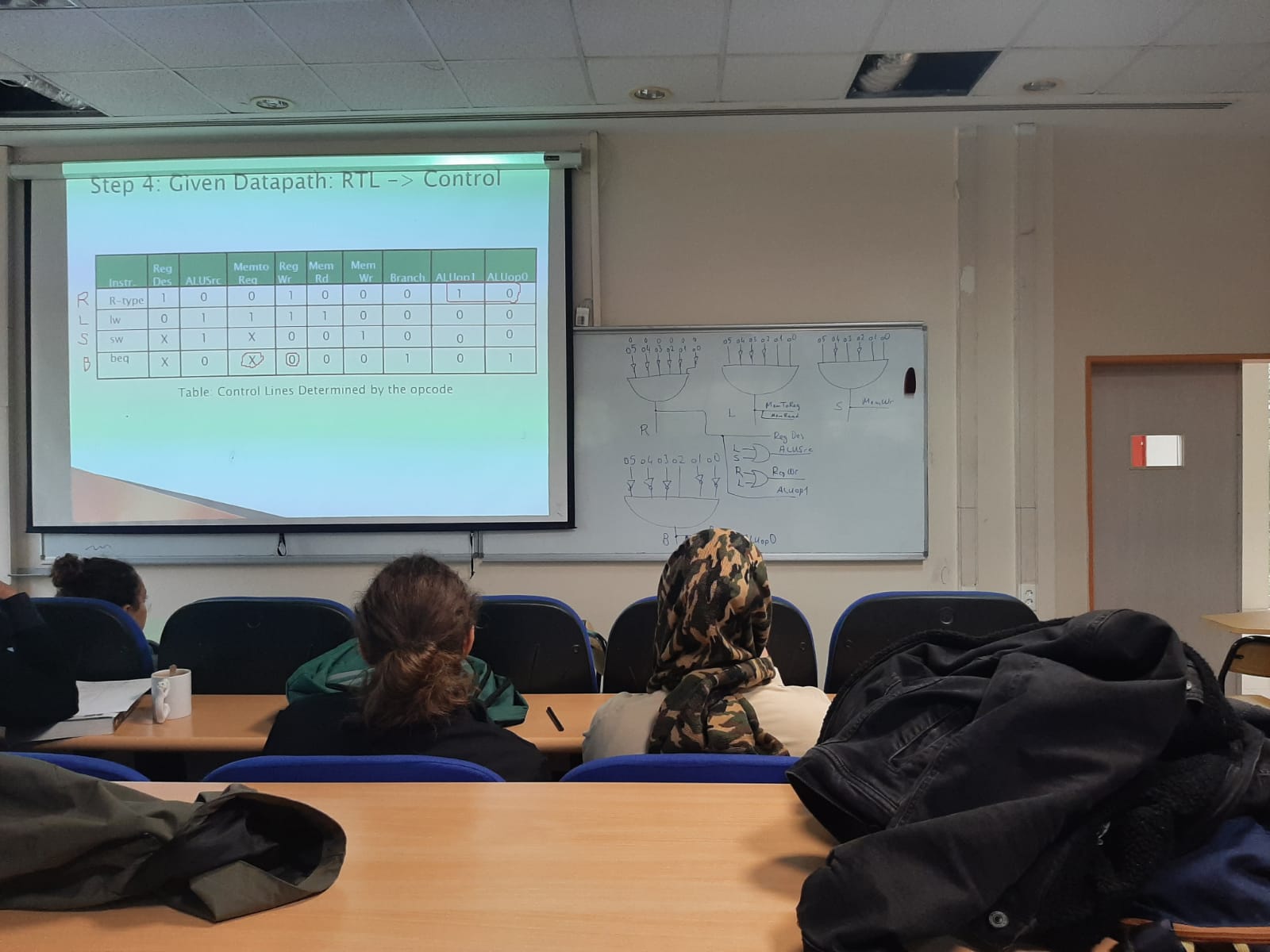
A picture containing diagram

Description automatically generated

The “Truth Table” for the Main Control

Table

Description automatically generated





Implementation of the Main Control

Diagram, schematic

Description automatically generated

Diagram, engineering drawing, schematic

Description automatically generated

An abstract view of the critical path – load instruction

Diagram, schematic

Description automatically generated

Dfetch + Dreg-read + Dmux + Dalu + Dmux = D (R-type) 🡪 50 ns diyelim CLK >= 50ns  
Dfetch + Dreg-read + Dalu + Dmem-read + Dmux = D (lw) 🡪 100ns diyelim CLK >= 100ns

Cycle period 100ns olmalı (slowest).